ELEC2032: Electronic Design
D3 - Analogue Design

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Abstract: A detailed account of Design, Simulation, Construction and Testing of the multi-stage amplifier circuit specified for ELEC2032: D3 Lab. Our overall circuit performed as expected from simulation giving a gain of 5.62 which is within the specifications. Input and output impedances were also within the required limits. The circuit fell short however at achieving a maximum swing at the output, with signals becoming distorted at an output of around $3V_{pk\text{-}pk}$, I believe this is due to the output bias of the 1st stage voltage amplifier being too high.

1. Introduction

The task set was to use technical knowledge gained in the first year to determine values for resistors and capacitors in a given circuit design for a multi-stage amplifier (figure *1.1*). The multi-stage amplifier uses two Motorola BC547 transistors to achieve both a voltage gain of 6 (with an acceptable error ±0.6) and a current gain at the final output.

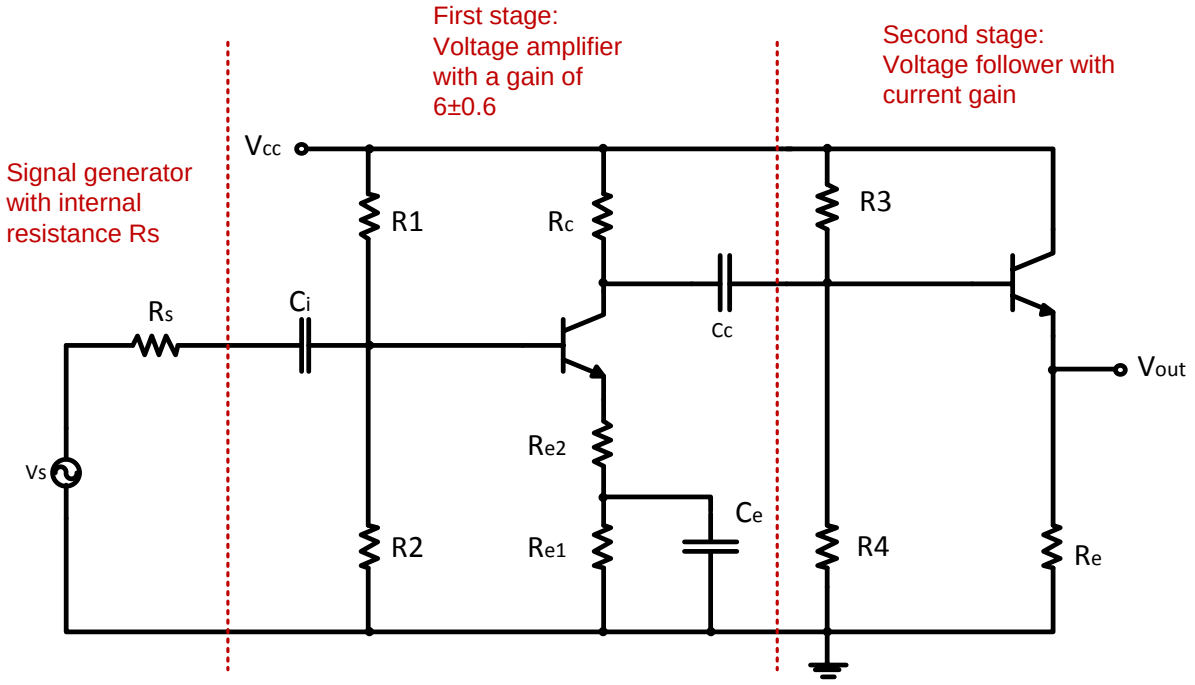


Figure 1.1: Multi-stage amplifier (Adapted from [1])

2. Theoretical Background and component value justification

2.1 Emitter follower (2nd stage) [2]

The emitter follower (figure *2.1.1*) is used to increase the current driving the output along with reducing the output impedance. This will allow the final multi-stage circuit to drive a load current with minimal signal loss. We chose to set the collector current of the follower to 1mA and as we required a maximum swing from the output ($V_o = V_{cc}/2 = 5V$) it would suggest a value of 5K is needed for R_e ($5/10^{-3} = 5000$). The BC547 transistor has a value of $V_{BE} = 0.55V$ to $0.7V$ when $V_{CE} = 5V$ so taking a mean value of V_{BE} to be 0.625V we deduced that the base of the transistor must be held at 5.625V in order to maintain maximum swing.

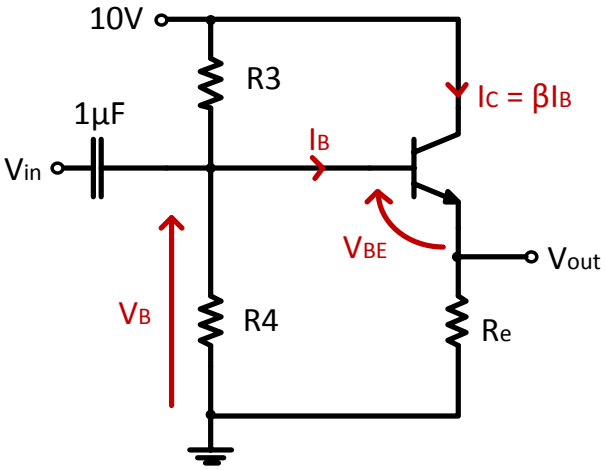


Figure 2.1.1: Emitter Follower

The resistors set in a potential divider configuration will produce the correct voltage at the base but the current must be enough to ensure βI_B is the 1mA needed for I_C. As β is 200 for I_C to be 1mA I_B needs to be 5µA. This is achieved by setting the current flowing through R3 and R4 to a value greater than (~10 times) required for I_B using (*2.1.1*). Specific values for each resistor can be found by setting the base voltage using R_4 (*2.1.2*).

$$I_{R3,R4} = \frac{V_{cc}}{R3 + R4} \tag{2.1.1}$$

$$R4 = \frac{V_{b2}}{I_{R3,R4}} \tag{2.1.2}$$

It can be seen from (*2.1.1*), (*2.1.2*) and by rounding R_e that satisfactory E12 values would be R3 = 150K, R4 = 220K and R_e = 4.7K. C_c is a coupling capacitor to enable biasing (1µF is a suitable value).

2.2 Emitter follower output impedance

The specification calls for the output impedance of the 2nd stage to be less than 150Ω. Using the Hybrid-Pi model (figure *2.2.1*) proves this is true.

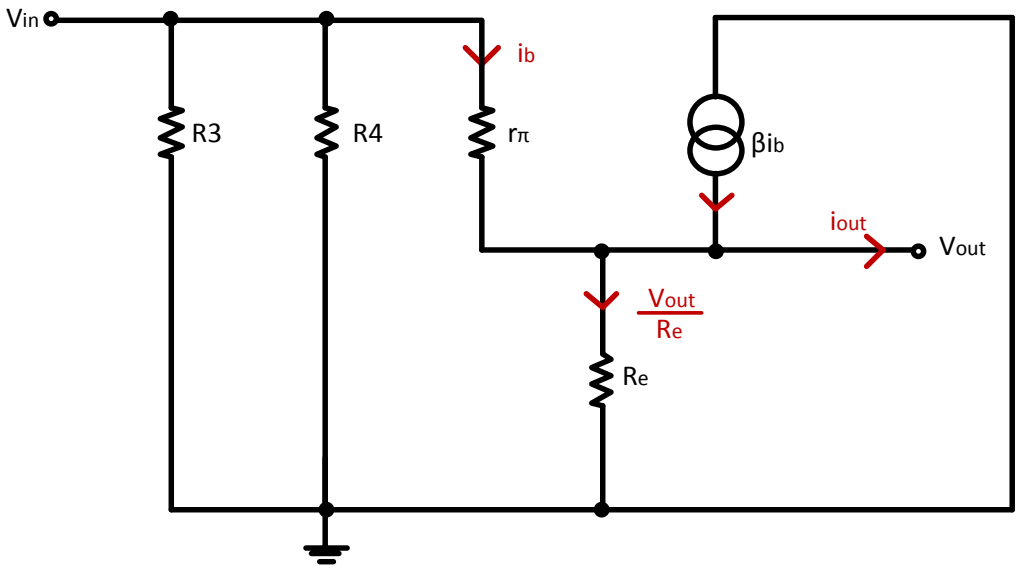


Figure 2.2.1: Hybrid-Pi model of the emitter follower

The circuit undergoes superposition so the supply rails can be short circuited. The transistor can also be considered as a resistor and current supply. Output impedance is found using equation *2.2.1*(substituted with equations *2.2.2* and *2.2.3*) resulting in equation *2.2.4*.

$$r_{out} = \frac{v_{out}}{i_{out}} \tag{2.2.1}$$

$$v_{out} = i_b r_\pi \tag{2.2.2}$$

$$i_{out} = i_b(\beta + 1) - \frac{v_{out}}{R_e} \tag{2.2.3}$$

$$\therefore r_{out} = \frac{1}{\frac{\beta + 1}{r_\pi} - \frac{1}{R_e}} \tag{2.2.4}$$

If $R_e >> 1$ and $\beta >> 1$ then equation *2.2.4* can be approximated to equation *2.2.5*

$$r_{out} \approx \frac{r_\pi}{\beta} = \frac{1}{g_m} \tag{2.2.5}$$

$$\frac{1}{g_m} = \frac{(\frac{KT}{q})}{I_c} \tag{2.2.6}$$

At room temperature and with I_c equal to 1mA the value of $r_{o2} = 25\Omega$ (equation *2.2.6*). This is much less than 150Ω and well within specification parameters.

2.3 Emitter follower input impedance

Using the same Hybrid-Pi model I used for the output impedance (figure *2.2.1*) equation *2.3.1* can be derived by considering current flow at the base and emitter of the transistor (remembering no current will be flowing from the output).

$$i_{in} = \frac{v_{in}}{r_\pi + (\beta + 1)R_e} + \frac{v_{in}}{R_3} + \frac{v_{in}}{R_4} \tag{2.3.1}$$

$$\therefore r_{in} = \frac{1}{\frac{1}{r_\pi + (\beta + 1)R_e} + \frac{1}{R_3} + \frac{1}{R_4}} \tag{2.3.2}$$

Substituting the chosen values of resistance and the derived value of r_π (equation *2.3.3*) the input impedance is calculated to be approximately 81.9KΩ (equation *2.3.2*).

$$r_\pi = \beta\frac{(\frac{KT}{q})}{I_c} = 5000 \tag{2.3.3}$$

2.4 Common emitter amplifier (1st stage) [3]

This is an inverting amplifier that gives the system a voltage gain. The signal at the input is passed through a coupling capacitor and biased using a potential divider at the base of the transistor. The current at the base determines the amplified current at the collector and because this is connected to the 10V supply the gain is negative (a rise at the input causes a drop at the output).

2.5 Common emitter amplifier gain

Using the Hybrid-Pi model also allows derivation of gain (figure *2.5.1*). The value of R_{e2} can be determined so the V_{out} is six times greater than any signal appearing at V_{in} (G = 6).

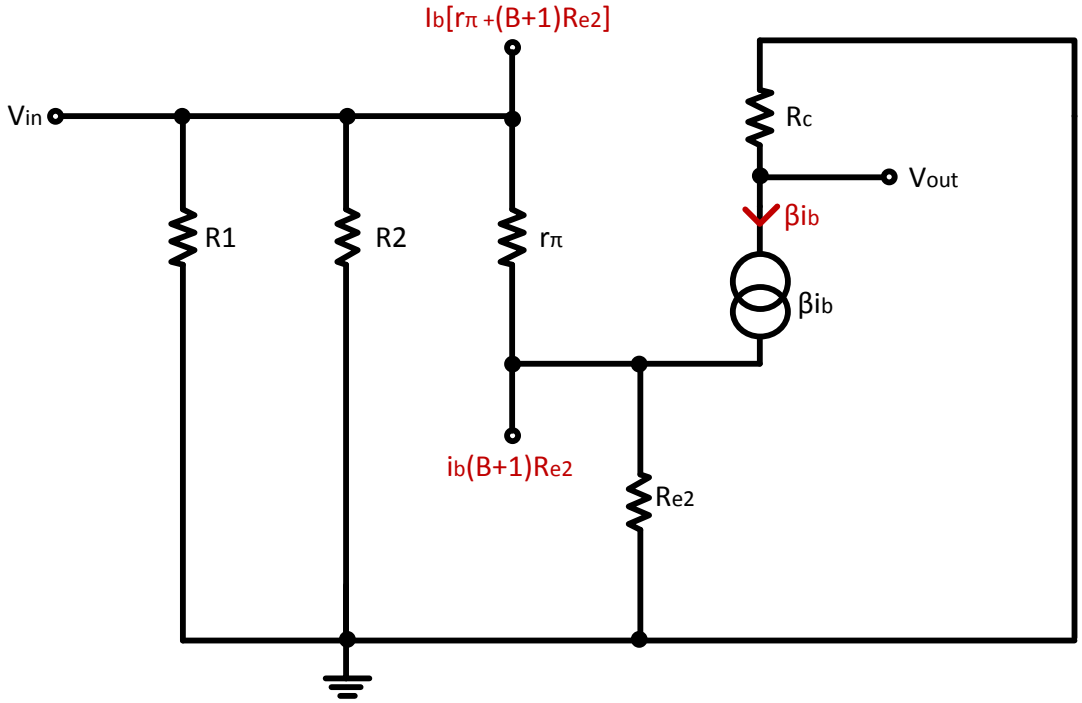


Figure 2.5.1: Hybrid-Pi model of the common emitter amplifier to derive gain

Voltages at the input and the output can be expressed as functions of current and resistances (*2.5.2* and *2.5.3*).

$$G = \frac{V_{out}}{V_{in}} \tag{2.5.1}$$

$$V_{out} = R_c \beta i_b \tag{2.6.2}$$

$$V_{in} = i_b[r_\pi + (\beta + 1)R_{e2}] \tag{2.5.3}$$

Gain (*2.5.1*) can then be expressed a function of resistances. Equation *2.6.4* is an approximation for gain and assumes $\beta >> 1$.

$$G \approx \frac{R_c}{\frac{r_\pi}{\beta} + R_{e2}} \quad (2.5.4)$$

The output requires maximum swing so I_c would need to be 1.06mA, knowing this current r_π can be found (as used in *2.3.3*) to be approximately 4.72KΩ. The value of R_{e2} is now a know value of 759.7Ω (the closest E12 values being 820Ω).

2.6 Common emitter amplifier output impedance [3]

To ensure the maximum possible percentage of the signal is passed from the 1st stage to the 2nd stage the impedances must be matched (signals should come out of low impedance and into high impedance). The input impedance has been found to be approximately 81.9KΩ so the output impedance of the first stage must be sufficiently less ($R_{o1} \leq 0.1R_{in2}$).

The impedance at the collector of a transistor is very high (> MΩ) and in this circuit configuration the output impedance is just R_c in parallel with impedance looking into the collector. The output impedance is therefore simply the value of R_c and setting this resistance to 4.7KΩ results in an output impedance of approximately 4.7KΩ.

2.7 Common emitter amplifier input impedance

The specification calls for an input impedance greater or equal to 40KΩ. Using the same Hybrid-Pi model from figure *2.6.1* the value of impedance going into the base of the transistor can be found making the total input impedance equation *2.7.1*.

$$r_{in} = R_1 || R_2 || [r_\pi + (\beta + 1)R_{e2}] \quad (2.7.1)$$

The value of β, r_π and R_{e2} are all know so the values chosen for R_1 and R_2 must satisfy equation *2.7.2*.

$$R_1 || R_2 \geqslant 53.6K\Omega \quad (2.7.2)$$

3. Simulation

Simulation of the circuit provides an accurate description of how it will perform in the physical world. I used OrCad to develop simulations for the gain of each stage separately, both stages combined and a frequency sweep of both stages.

3.1 Simulation of 1st stage gain

3.2 Simulation of 2nd stage gain

3.3 Simulation of multi-stage amplifier

3.4 Simulation of the frequency response of the multi-stage amplifier

4. Methods of Measurement

The method of attack for measuring the system is building each stage and testing it individually then concatenating the stages to produce a multi-stage amplifier that should pass all specifications. Any AC signal used for testing are 1KHz unless stated otherwise.

4.1 Measuring Gain

To measure the gain of an AC amplifier means passing an AC signal (in this case a sine wave) through the amplifier then using an oscilloscope to compare the voltage amplitude at both the input and the output (figure *4.1.1*).

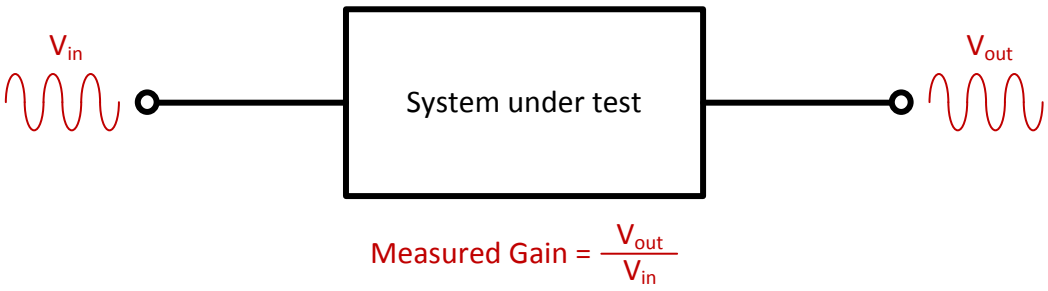


Figure 4.1.1: Gain testing setup

4.2 Measuring the gain of the 2nd stage

This stage is just an emitter follower so no gain is expected. Figure *4.2.1* shows this is true because the input and output signals both have amplitude of $1.54V_{pk\text{-}pk}$.

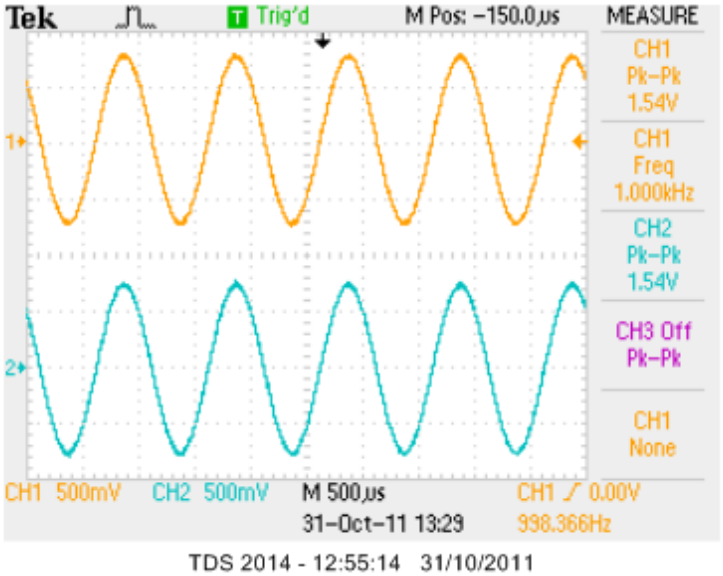


Figure 4.2.1: Input signal (Blue) and output signal (Yellow) of the 2nd stage

4.3 Measuring the gain of the 1st stage

This stage provides the voltage gain for the whole system. It needs to be 6±0.6 to pass the specifications.

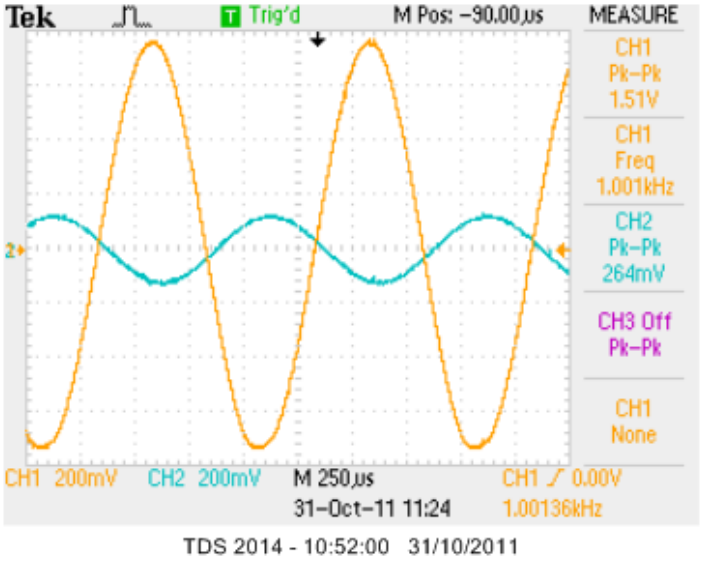


Figure 4.3.1: Input signal (Blue) and output signal (Yellow) of the 1st stage

The oscilloscope trace (figure *4.3.1*) shows a gain of -5.72 which is acceptable.

4.4 Measuring Impedance

Measuring impedance (although measured in Ohms) can't be done with an Ohm meter because it is a complex quantity. Measuring the magnitude requires another impedance of a known value but is as close as possible to the value of the unknown impedance (estimated through theory). These are then placed in potential divider configuration (figure *4.4.1*) and by comparing the signal degeneration of a sine wave at the output a value for the unknown impedance can be found. A coupling capacitor is also used to remove any DC offset.

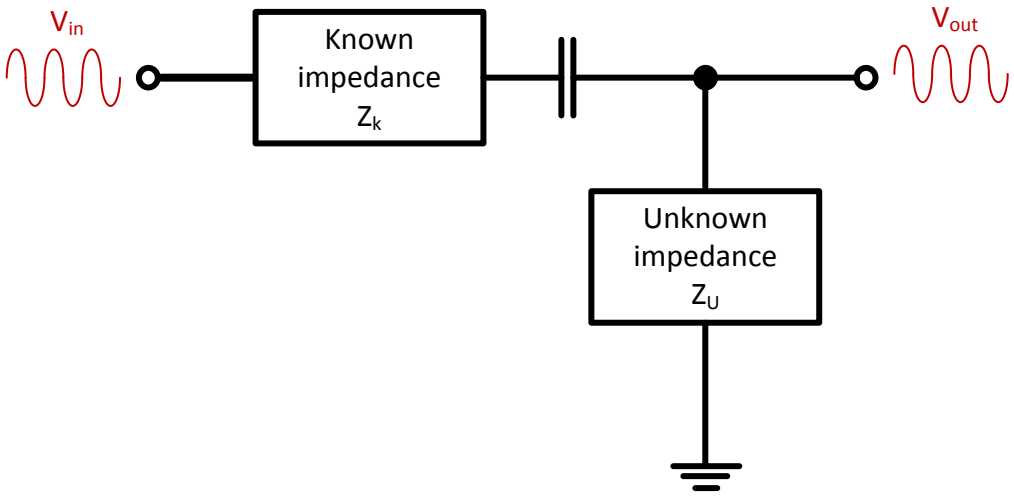


Figure 4.4.1: Measuring an unknown impedance

Depending on whether the input or output impedance is being measured the position of the known and unknown impedances will swap. After finding the gain (G < 1) the unknown impedance will either be found using equation *4.4.1* (input impedance: same as in figure *4.4.1*) or equation *4.4.2* (output impedance: impedances swapped in figure *4.4.1*).

$$Z_u = \frac{GZ_k}{1-G} \tag{4.4.1}$$

$$Z_u = \frac{Z_k(1-G)}{G} \tag{4.4.2}$$

4.5 Input impedance of the 1st stage

Using a 40KΩ resistor as the known impedance the value of the input impedance of the first stage was calculated to be 42KΩ (figure *4.5.1*).

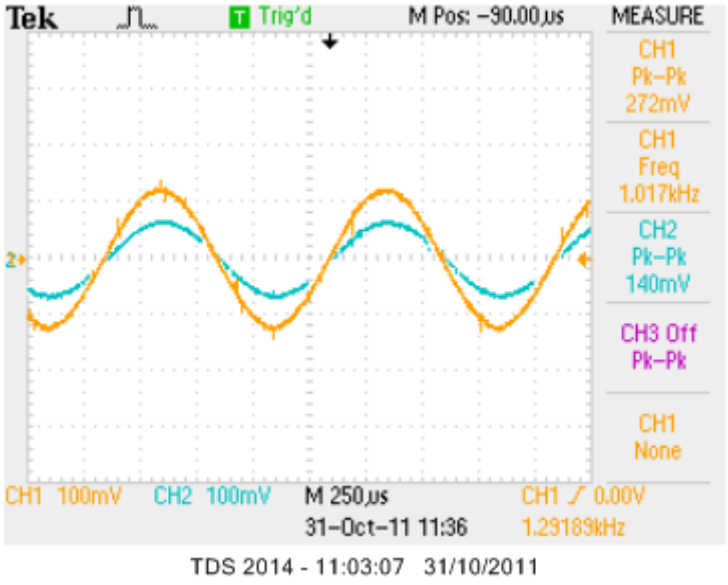


Figure 4.5.1: Input signal (Yellow) and output signal (Blue) of the known impedance

4.6 Output impedance of the 1st stage

This result (although passing the specification) was unexpectedly low, I had calculated the output impedance to be approximately the same value as the resistor at the collector, the measured value of 310Ω is less than a tenth of the expected impedance of 4.7KΩ.

I cannot see any mistake in my theoretical calculations so I must have to attribute this low reading to a mistake in practical measurement (I discuss this problem more in section *5.Conclusions*).

4.7 Input impedance of the 2nd stage

Using a 47KΩ resistor as the known impedance the value of the input impedance of the second stage was calculated to be 84.6KΩ (figure *4.7.1*).

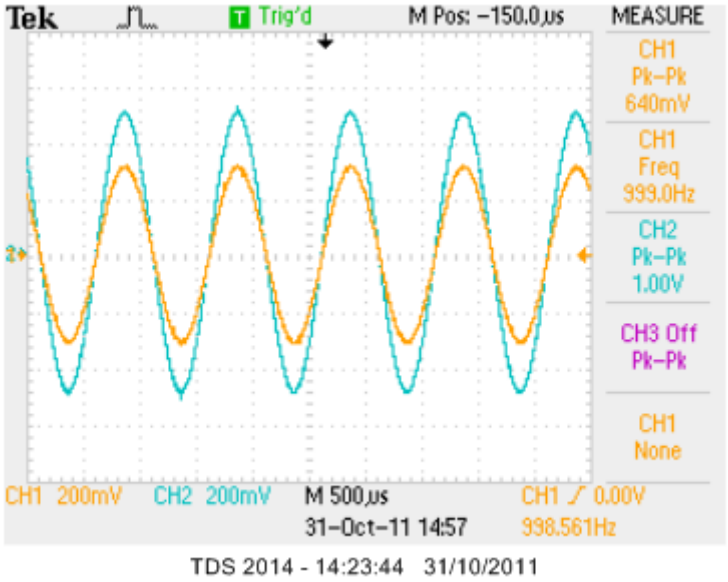


Figure 4.7.1: Input signal (Blue) and output signal (Yellow) of the 2nd stage

4.8 Output impedance of the 2nd stage

Using a 150Ω resistor as the known impedance the value of the input impedance of the second stage was calculated to be 85Ω (figure *4.8.1*).

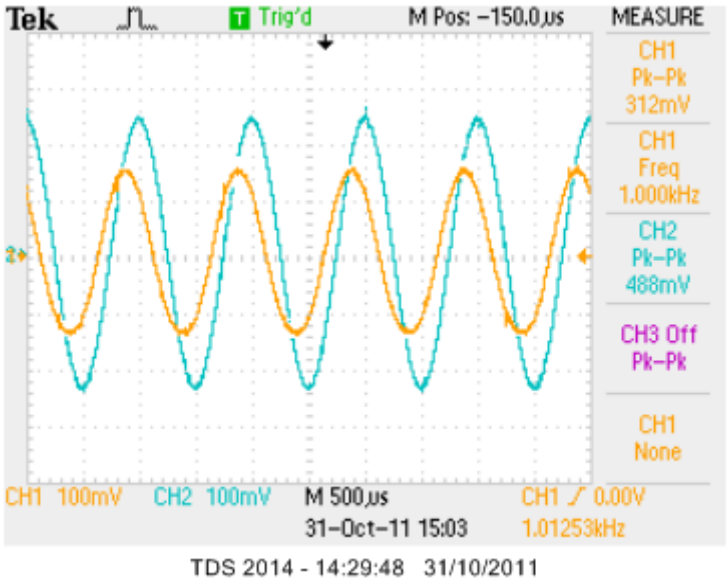


Figure 4.8.1: Input signal (Blue) and output signal (Yellow) of the known impedance

4.9 Multi-stage measurements

Using the same techniques as used on the individual stages the full system had…

- A gain of 5.62
- An input impedance of 50.7kΩ
- An output impedance of 110Ω

These fell within the specifications but the circuit build did not achieve maximum swing (I discuss this problem more in section *5.Conclusions*).

4.10 Experimenting with the bypassing capacitor (C_E)

This capacitor bypasses R_{e1} when an AC signal is passing through the amplifier but at DC it does not so the emitter resistance is R_{e1} + R_{e2}. Removing the capacitor means that R_{e1} is never bypassed so the emitter resistance is higher for AC conditions and from section 2.6 it can be see the gain is affected by this. A higher emitter resistance means a reduced gain. In fact it was reduced to just 1.15 (figure *4.10.1*).

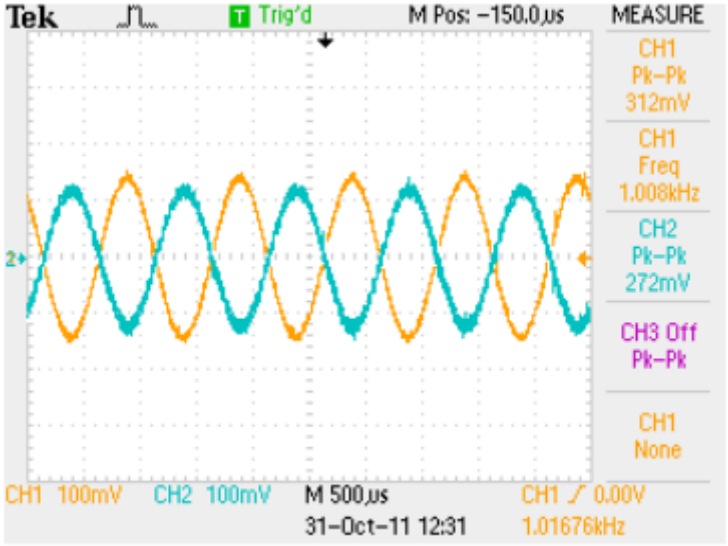
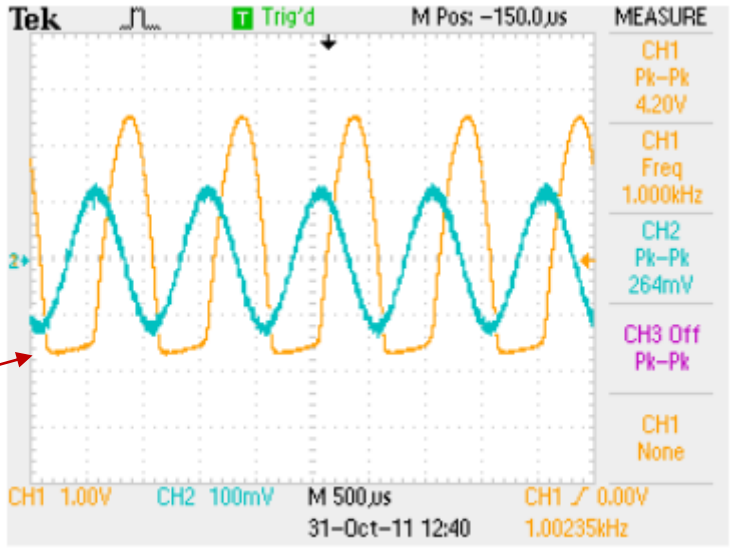


Figure 4.10.1: Input signal (Blue) and output signal (Yellow) of the 1st stage circuit with C_E removed

Using the capacitor instead to bridge the resistors at the emitter means the resistance is lower and hence the gain is greater. The gain in this case (G = 15.91) is so high the output becomes distorted because the supply cannot provide a high enough voltage (figure *4.10.2*).

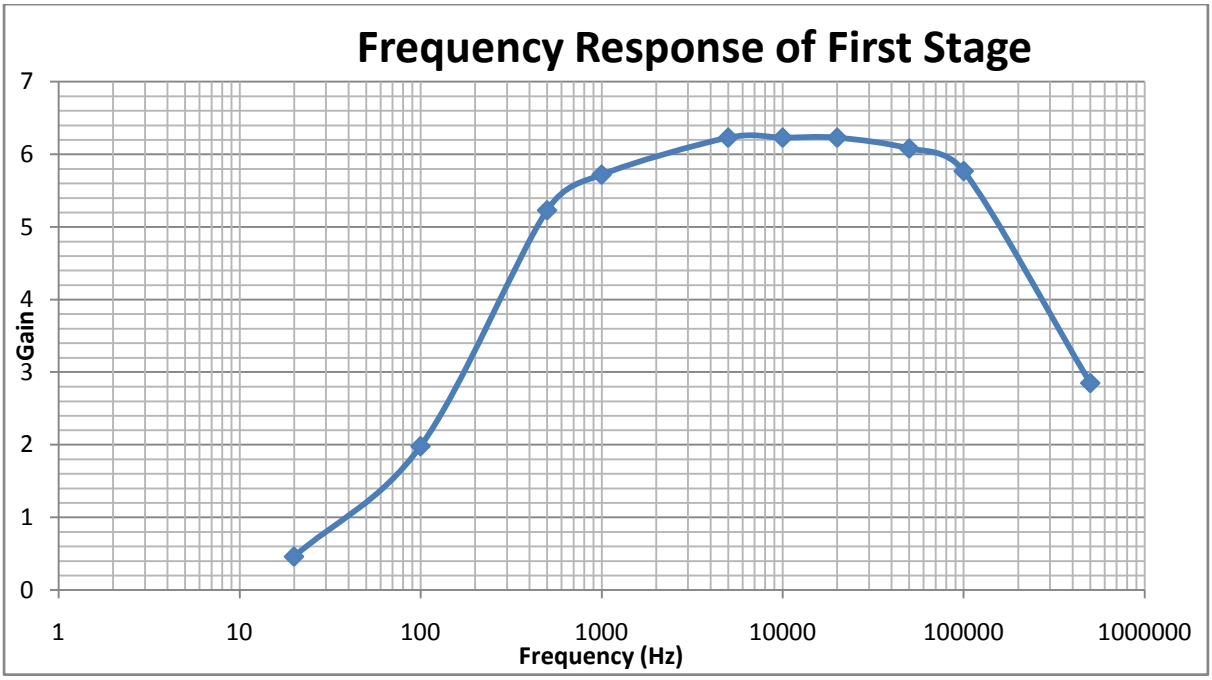


Distortion of the sine wave

Figure 4.10.2: Input (Blue) and output (Yellow) signals of the 1st stage circuit when C_E bridging R_{e1} and R_{e2}

4.11 Frequency response of the 1st stage [4]

After scanning through frequency in



5. Conclusions

The circuit I produced passed four out of the five parameters and overall was a success however its behaviour was unexpected in two areas…

1. The output signal would distort when reaching approximately $3V_{pk\text{-}pk}$ therefore failing specification "5. The output voltage should have the maximum swing" [1]
2. The output impedance of the 1st stage was much less than expected

6. References

[1] Dr. Sasan Mahoodi, "D3 Analogue Design", University of Southampton, https://secure.ecs.soton.ac.uk/notes/elec2032/D3/D3CourseWork.pdf

[2] Richard R. Spencer, Mohammed S. Ghausi, "Introduction to Electronic Circuit Design", Pearson Education Inc, 2003, pp. 416-429

[3] Paul Horowitz, Winfield Hill, "The Art of Electronics", Cambridge University Press, 2nd edition, 1989, pp 76-88

[4] Website: http://hyperphysics.phy-astr.gsu.edu/hbase/electric/impc.html